FPGA Based Three Phase Multilevel PWM Inverter

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Abstract-- **This paper presents, a phase shifted carrier pulse width modulation is proposed, which can minimize the output total harmonic distortion and enhances the output voltages from five level inverter to multilevel topologies. Multilevel inverters are important for power electronics applications such as flexible AC transmission systems, renewable energy sources, unin terruptible power supplies and active power filters. Two novel methodologies adopting the phase shifted carrier pulse width modulation concept are proposed in this paper. The phase shifted carrier pulse width modulation cascaded multilevel inverter strategy minimized output total harmonic distortion and phase shifted carrier switching frequency optimal pulse width modulation cascaded multilevel inverters strategy enhances the output voltages. Field programmable gate array has been chosen to implement the pulse width modulation due its fast proto typing, simple hardware and software design. Simulation and Experimental results are provided.**

Keywords- Phase shifted pulse width modulation; Switching frequency optimal pulse width modulation; Total harmonic distortion; Output voltage; Cascaded Multilevel inverter.

I. INTRODUCTION

For increasing use in practice and fast developing of high power devices and related control techniques, multilevel inverters have become more attractive to researches and industrial companies [1]. Multilevel inverters have achieved an increasing contribution in high performance applications [2]-[5]. The control objective is to compare reference and phase shifted carrier wave using three phase five level cascaded inverter[6],[8]. The multilevel inverter advantages are improved output voltage, reduced output total harmonic distortion, reduced voltage stress on semiconductors switches and decreases of EMI problems[6],[9].

The different multilevel inverter structures are cascaded H-bridge, diode clamped and flying capacitors multilevel inverters. Increasing the number of levels in the inverter without requiring high ratings on individual devices can increases the power rating [10]. Two novel phase shifted carrier pulse width modulation schemes are present which take advantage of special properties available in multilevel inverter to minimize total harmonic distortion and increases output voltage [14].

II. THREE PHASE CASCADED MULTILEVEL INVERTER

A Field programmable gate array based three phase structure of five level cascaded inverter is illustrated in Fig. 1

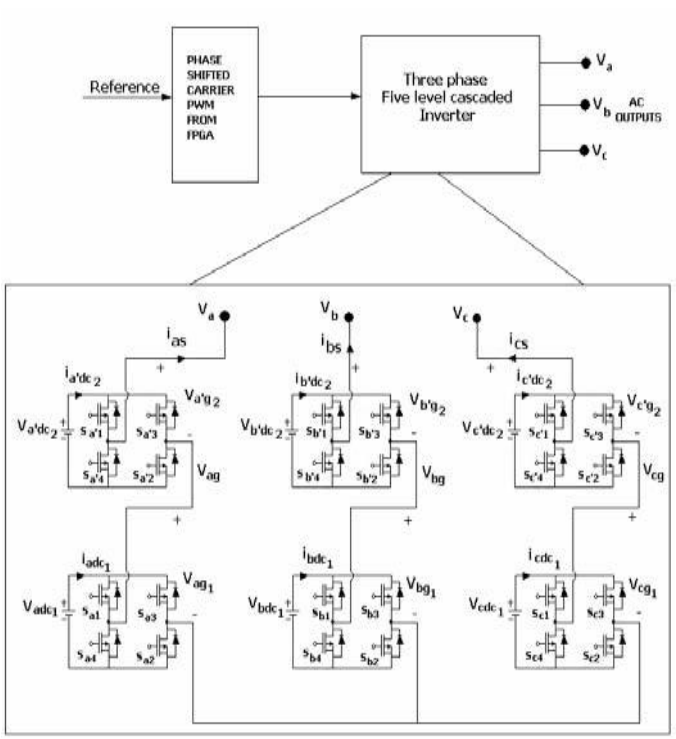

Figure 1. FPGA based three phase cascaded five level inverter

Each dc source is connected to a three phase inverter. Each inverter level can generate three different voltage outputs, +Vdc, 0, and –Vdc by connecting the dc source to the ac output by different combinations of the four switches. The ac outputs of each of the different full bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascaded inverter is defined by m=2s+1, where s is the number of separate dc sources.

III. PHASE SHIFTED CARRIER PULSE WIDTH MODULATION (PSC PWM)

Fig. 2 shows the Phase shifted carrier pulse width modulation. Each cell is modulated independently using sinusoidal unipolar pulse width modulation and bipolar pulse width modulation respectively, providing an even power distribution among the cells. A carrier phase shift of 180°/m for cascaded inverter is introduced across the cells to generate the stepped multilevel output waveform with lower distortion.

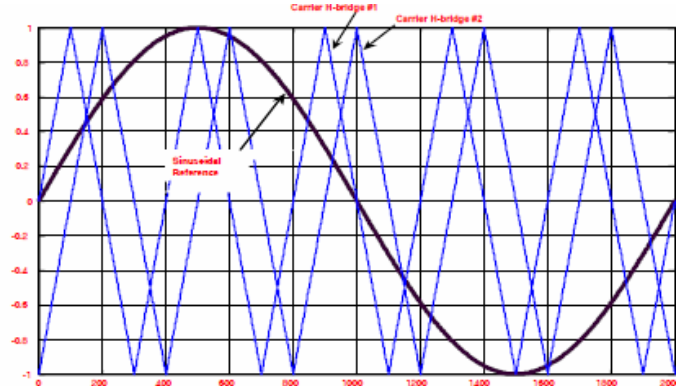

Figure 2. Phase shifted carrier pulse width modulation

IV. RESULTS

The table.1 shows THD and output voltage value for PSC PWM and PSC-SFO PWM. When modulation Index is more than 1, it is called as over modulation and if it's below or equal to 0.5 then it is called low modulation Indices.

TABLE I. OUTPUT VOLTAGE AND THD FOR PSC PWM AND PSC-SFO PWM

Modulation Index	PSC PWM		PSC-SFO PWM	
	THD%	Vac	THD%	Vac
1.1(over modulation)	3.75	10.65	21.03	11.86
1.0	0.75	10.15	20.92	11.43
0.9	0.35	10.01	20.65	11.02
0.8	1.05	9.36	20.51	10.04
0.7	2.45	8.58	20.72	9.32
0.6	4.60	6.32	21.02	7.82
0.5(Low modulation)	6.83	5.03	21.24	5.04

A. Simulation Results

To verify the proposed schemes, a simulation model for a three phase five level cascaded H-Bridge inverter is implemented. The simulation parameters are as following 5KW rating, three phase load R = 100 ohms, L = 20mH, each source Vdc = 5V, switching frequency 5KHz. Diagrams of the phase leg voltages have been calculated and drawn for PSC PWM in fig 3,4.

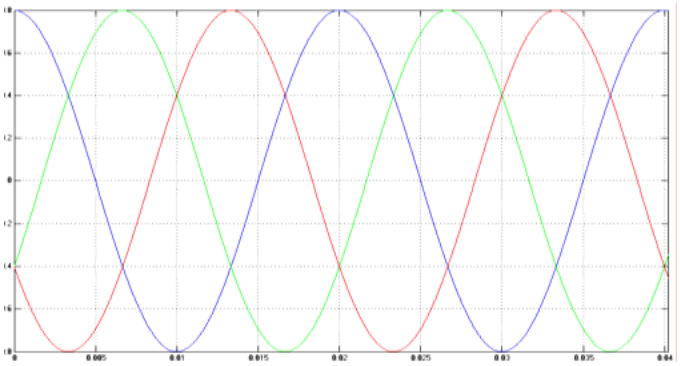

Figure 3. PSC PWM modulating signal

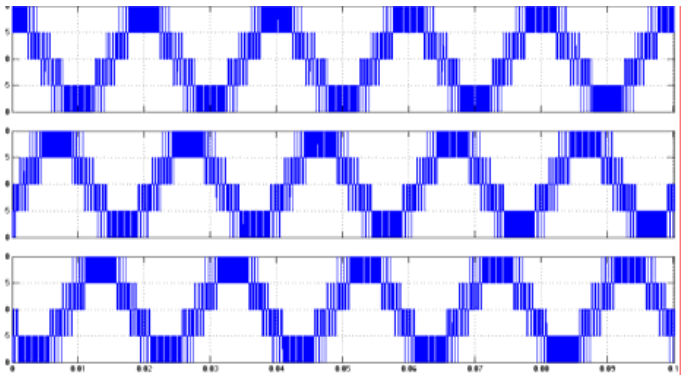

Figure 4. PSC PWM output voltage (Modulation index 0.9)

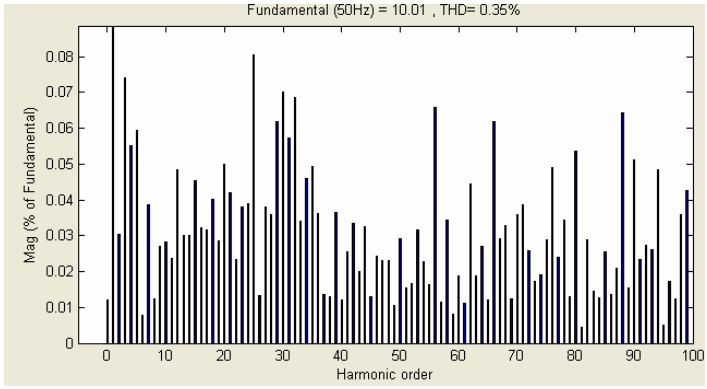

Figure 5. PSC PWM Harmonic spectrum (Modulation index 0.9)

Fig. 4 and Fig. 5 shows the output voltage of PSC PWM with modulation index 0.9, fundamental frequency 50Hz and THD value is 0.35% with output voltage of 10.01V. Fig. 7shows the output voltage and harmonic spectrum with modulation index 1.1. The THD value is 3.84% with output voltage of 10.65V. Fig.6 shows the output voltage and harmonic spectrum with modulation index 0.5. The THD value is 6.83% with output voltage of 5.039V.

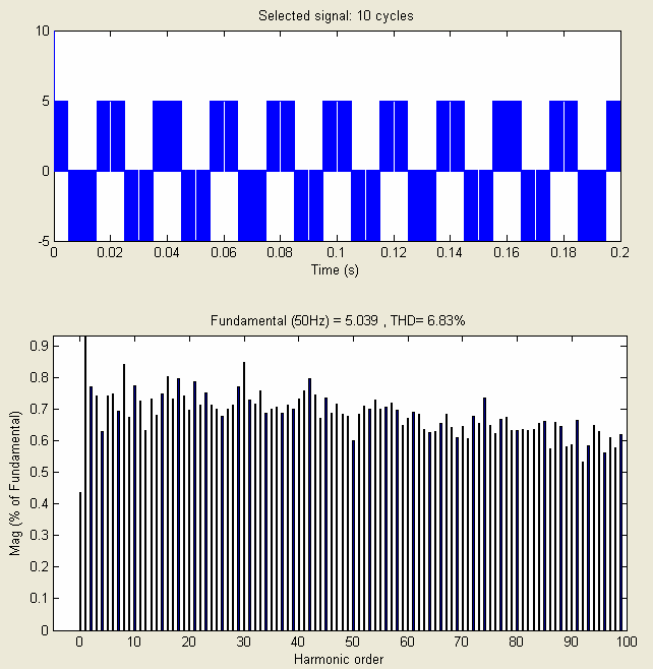

Figure 6. PSC PWM output voltage and harmonic spectrum (Modulation index 0.5)

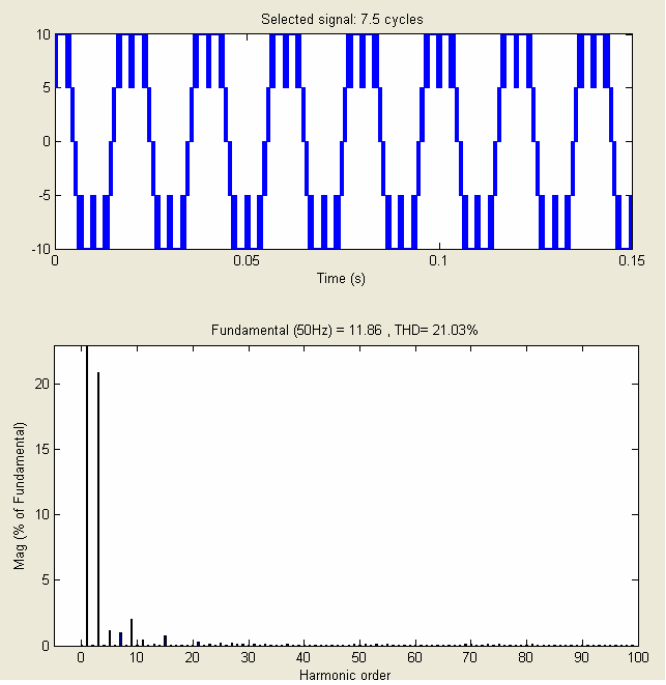

Figure 7. PSC-SFO PWM output voltage and harmonic spectrum (Modulation index 1.1)

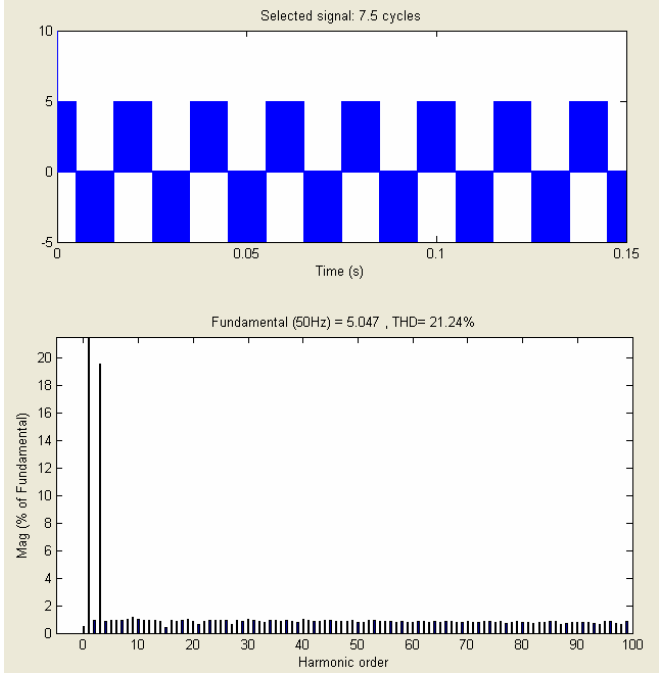

Figure 8. PSC-SFO PWM output voltage and harmonic spectrum (Modulation index 0.5)

B. Hardware Results

A hardware setup of three phase five level cascaded inverter has been built to validate the theoratical analysis. The hardware parameters are as following, 5KW rating, three phase load R = 100 ohms, L = 20mH, each source Vdc = 5V, fundamental frequency 50HZ, switching frequency 5KHZ and Xilinix Spartan – DSP controller (FPGA). The three phase output voltage waveform for PSC PWM method shown in fig. 9 and PSC-SFO PWM method shown in Fig.1.

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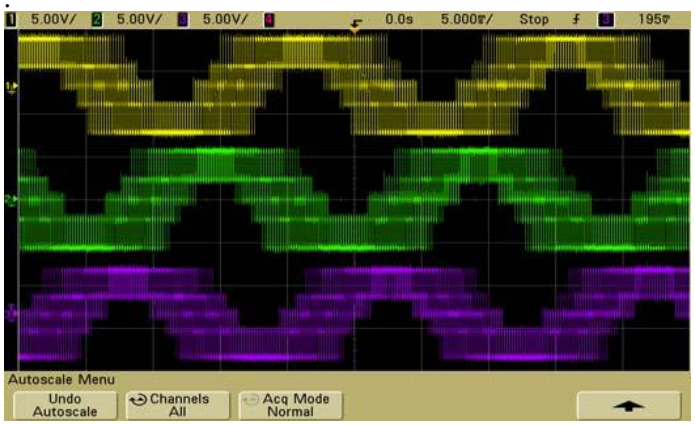

Figure 9. PSC PWM output voltage

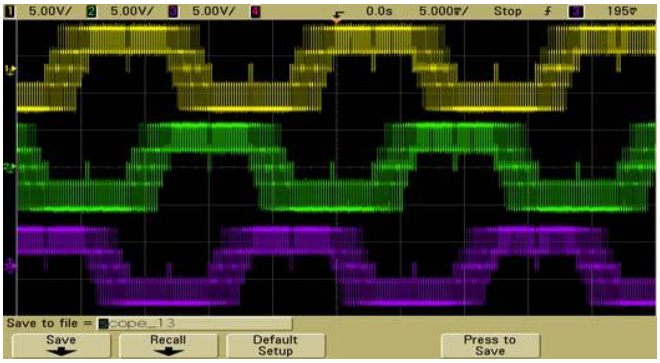

Figure 10. PSC-SFO PWM output voltage

Figure 11. Hardware setup of three phase cascaded multilevel inverter

V. RESULTS

In this paper, two new schemes adopting the phase shifted pulse width modulation concept are proposed. The PSC PWM strategy reduces the THD and PSC-SFO PWM strategies enhances the fundamental output voltage. The multilevel inverter improves output voltage, reduces output total harmonic distortion and voltage stress on semiconductors switches. By adopting PSC PWM strategy with modulation index equal to 0.9, the THD value is reduced to 0.35 and output voltage is obtained to 10.01V. To increase the output voltage value to 11.01V, PSC-SFO PWM strategy is used. Those schemes confirmed by simulation results and experimental results.

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